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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,549	07/19/2006	**Henry Tan**	P/2778-84	6234

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EXAMINER	
YU, JAE UN	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,549	TAN ET AL.	
	Examiner	Art Unit	
	JAE U. YU	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/3/08*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-20* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The examiner acknowledges the applicant's submission of an amendment dated 12/3/2008. At this point, claims 1-20 have been amended. Thus, claims 1-20 are pending in the instant application.

Response to Amendment

In view of the applicant's amendment, the 35 USC 112 rejection for claim 5 is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-5 and 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban (US 5,404,485) in view of Higuchi et al. (US 2002/0120820), referred to as "Higuchi" hereinafter.

2. As per **independent claim 1**, Ban discloses; "a data interface for transferring data packets into and out of the portable storage device, an interface controller, a master control unit, and a flash memory unit configured to incorporate the physical address regions, the interface controller being operable to send data received through

the data interface to the master control unit, and the master control unit being operable to recognize a data packet received by the data interface as encoding one of a READ instruction indicating a logical address and a WRITE instruction indicating the logical address and data to be written: **[Figure 1 & Figure 6]**",

"upon receiving the READ instruction, to access the memory address mapping table **[Figure 3]**, to read data from a first physical address in the memory unit **["Physical Address", Figure 5]** corresponding, according to the memory address mapping table, to the logical address **["Virtual Address", Figure 5]**, and to transmit to the data interface one or more data packets including the data read", and

"upon receiving the WRITE instruction, to determine, as a first determination, whether the first physical address is in an erased state **[Step 47, Figure 6]** and: when a result of the first determination is affirmative, to write the data to be written the physical address **[Step 49, Figure 6]**, and when the result of the first determination is negative, to modify the memory address mapping table in accordance with a block queue list one or more queuing physical address regions **[free addresses listed in unit allocation table, Figure 6]** to thereby associate a second physical address with the logical address **[Step 53 & 54, Figure 6]**, the second physical address belonging to a queuing physical address region at a head of the block queue, to write the data to be written to the second physical address **[Step 52, Figure 6]**, and to copy any data stored in other potions of a first physical address region designated by the first physical address to

corresponding locations of a second physical address region designated by the second physical address **[Figure 7 & 8]**".

Ban does not disclose expressly that the flash memory unit is a "NAND flash memory".

Higuchi discloses a NAND flash memory in paragraph 7.

Ban and Higuchi are analogous art because they are from the same field of endeavor of flash memory control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Ban by including a NAND flash memory as taught by Higuchi in paragraph 7.

The motivation for doing so would have been "a large capacity, small size, and low power consumption" as expressly taught by Higuchi in paragraph 7.

3. As per **claim 2**, "wherein the memory address mapping table is stored as mapping data in the NAND flash memory unit **[map stored in the flash memory, Paragraph 3]**, the master control unit being operable to modify the mapping data upon modifying the memory address mapping table **[Figure 3 & 6]**".

4. As per **claim 3**, "the memory control address unit operable upon being initiated, to extract the mapping data from the NAND flash memory unit **[map stored in the flash memory, Paragraph 3]** and generate the memory address mapping table within RAM memory **[map stored in random access memory, Paragraph 3]**".

5. As per **claim 4**, "the portion of the mapping data defining the mapping between a respective physical address region and a logical address region is stored within that the respective physical address region **[Figure 3]**".

6. As per **claim 5**, "the mapping data relating to the respective physical address region is stored in a control data storage sector of one or more pages of the respective physical address region **[Figure 3]**".

7. As per **claim 9**, "each physical address region is a respective block of the NAND flash memory unit **[Figure 3]**".

8. As per **claim 10**, "the physical address regions comprise groups of blocks in the NAND flash memory unit, the groups being defined to a grouping table **[Figure 9]**".

9. As per **claim 11**, "the majority of the groups of blocks is defined in the NAND flash memory unit according to a rule, and the grouping table defines groups positioned in the NAND flash memory unit according to exceptions to the rule **[Figure 9]**".

10. As per **claim 12**, "the memory address mapping table contains a flag for any logical address associated with one of the groups of blocks positioned according to the exceptions to the rule **[Figure 9]**".

11. As per **claim 13**, "the master control unit associates consecutively following logical addresses within a logical address region **[Element 31, Figure 4]** with respective pages in different ones of the blocks **[Element 35, Figure 4]**".

12. As per **claim 14**, "the master control unit associates consecutive logical addresses into sets **[Element 31, Figure 4]**, each of the sets having a number of members equal to the number of blocks in each group, and for each given set the master control unit associates the logical addresses of that set with corresponding pages of the respective blocks **[Element 35, Figure 4]**".

13. As per **claim 15**, "the master control is operable, in response to receiving a first WRITE instruction to implement the first WRITE instruction only upon determining that **[receiving a first write instruction, Figure 6]**, within a predefined period, a second WRITE instruction obeying a predefined similarity criterion is not received **[no second instruction received, Figure 6]**".

14. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban (US 5,404,485) in view of Higuchi et al. (US 2002/0120820) as applied to claim 1 above and further in view of Crawford et al. (US 5,918,055), referred to as "Crawford" hereinafter.

15. As per **claim 6**, Ban and Higuchi disclose the device recited in claim 1.

Ban and Higuchi do not disclose expressly the first physical address is placed at the rear of the block queue.

Crawford discloses transferring a token value to a "valid-request-queue" in the abstract.

Ban, Higuchi and Crawford are analogous art because they are from the same field of endeavor of memory access control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Ban and Higuchi by implanting the token scheme as taught by Crawford in the abstract.

The motivation for doing so would have been the simpler system design as expressly taught by Crawford in column 2, lines 7-10.

16. As per **claim 7**, "the physical address regions listed on the block queue are in the erased state **[Figure 6]**".

17. As per **claim 8**, "reserved physical address regions **["Transfer Unit", Figure 7]** which cannot become associated with the logical address under an operation of the master control unit when modifying the memory address mapping table".

17. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban (US 5,404,485) in view of Higuchi et al. (US 2002/0120820) as applied to claim 1-15 above, and further in view of Horn et al. (US 2005/0050273), referred to as "Horn" hereinafter.

18. As per **claims 17 and 18**, Ban and Higuchi disclose the device recited in claim 15.

Ban and Higuchi do not disclose expressly that if two write commands try to access the same memory location, then directs a command to other memory location.

Horn discloses such two write instructions, wherein each instruction is directed to a different memory location from one other in the abstract.

Ban, Higuchi and Horn are analogous art because they are from the same field of endeavor of memory access control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Ban and Higuchi by holding multiple requests in a queue when the requests cause an access overlap as taught by Horn in the abstract.

The motivation for doing so would have been to alleviate memory access conflicts as expressly taught by Horn in the abstract.

19. As per **claim 19**, "the WRITE instruction relates to a plurality of said selected logical addresses **[Figure 3 & 4, Ban]**".

20. As per **claim 20**, "a pattern recognition unit operable to recognize as a high frequency logical address a logical address encoded in WRITE instructions that is received with high frequency **[access conflict, Abstract, Horn]**, and to set said high frequency logical address as said selected logical address **[Figure 3 & 4, Ban]**".

Arguments Concerning Prior Art Rejections

1st Point of Argument

Regarding claim 1, the applicant argues that the cited prior arts fail to teach queuing physical memory regions. The examiner interprets such queue as a list of free memory regions. Since Ban discloses associating physical memory regions with corresponding logical addresses in Figures 3 and 4 and listing free memory regions in unit allocation tables as depicted in Figure 7, Ban clearly anticipates the claimed queuing action.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

A. Subject Matter Considered Allowable

1. **Claim 16** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

2. The primary reasons for allowance of **claim 16** in the instant application is the combination with the inclusion in the claim that **"following a modification of the memory address mapping table in relation to a first logical address, and prior to**

said copying of the data from the first physical address to the second physical address, said similarity criterion is whether the second WRITE instruction relates to a logical address corresponding to a location designated by the first logical address of the data to be copied, and when the similarity criterion is satisfied, aborting said copying operation and instead writing data specified by the second WRITE instruction to the second physical address". The prior art of record neither anticipates nor renders obvious the above recited combination.

3. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

B. Claims Rejected in the Application

Claims 1-15 and 17-20 have received a second action on the merits and are subject of a second action final.

C. Direction of Future Remarks

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Un Yu who is normally available from 9:00 A.M. to 5:30 P.M. Monday thru Friday and can be reached at the following telephone number: (571) 272-1133.

If attempts to reach the above noted examiner by telephone are unsuccessful, the Examiner's supervisor, Sanjiv Shah, can be reached at the following telephone number: (571) 272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jae U Yu/

Examiner, Art Unit 2185

1/20/2009

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185